Photonic Integration

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1. Introduction

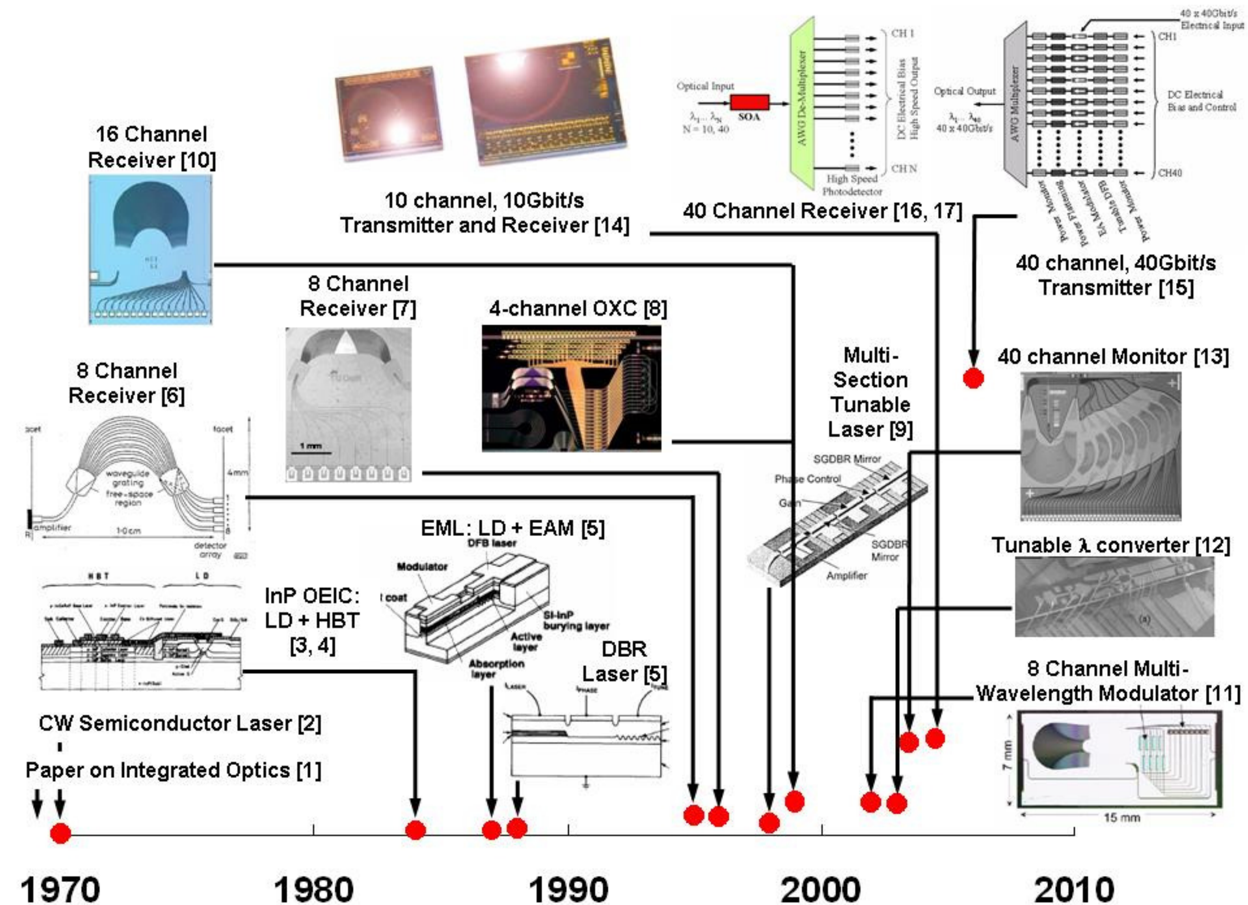

Fig. 1: Historical trend and timeline for Photonic Integration

Photonic integration has a very long history dating back to the original paper by Miller in 1969 [1]. It is interesting to note that this paper predates the first CW semiconductor laser [2]. Fig. 1 traces the history of photonic integration from the perspective of active components integrated onto an InP substrate [3-17]. The red points on the chart refer to the progression in the number of components integrated onto a single InP substrate on a linear scale from 1 for the single channel devices to over 240 for the 40 channel, 40Gbit/s per channel transmitter at the top right hand corner.

In the following section we will first give a historical overview of the development of complex Photonic ICs, up to the Large Scale PICs that have been developed by Infinera and that we consider as a breakthrough in the application of complex PICs. In Sec. 3 we present some details of these complex PIC's. Next we discuss how photonic integration can address the needs of ever increasing data capacity (Sec. 4), increasing functionality (Sec. 5) and increasing integration scale (Sec. 6).

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2. Historical Overview (Refs are in Fig, 1)

For the first decade or so after the demonstration of the CW laser in the GaAs system, lasers in the InP started to mature. In mid 1980's there was active work in the area of Opto-Electronic Integrated Circuits (OEIC) where the integration of electronic devices like HBT (heterojunction bipolar transistor) and FET (field effect transistor) with laser diodes and photodetectors were pursued. In the late 1980's three section tunable DBR (Distributed Bragg Reflector) lasers were introduced. This was also when electro-absorption modulators (EAM) integrated with DFB lasers were demonstrated. The trend continued with more complicated (four and five section) tunable laser sources which were also integrated with an EAM or a semiconductor optical amplifier (SOA). The next step was the demonstration of the Arrayed Waveguide Grating (AWG) or PHASAR (Phased Array) router integrated with photodetectors for multi-channel receivers or with gain regions and EAM for multi-frequency lasers and multi-channel modulated sources. One of the most complex PICs reported in the last century was a 4-channel optical cross-connect integrating 2 AWGs with 16 MZI-switches. At this stage the most sophisticated laboratory devices still had component counts below twenty while those in the field had component counts of about four.

The trend in low level photonic integration continued into the first few years of the twenty first century. First steps towards a larger integrated chip were announced in 2003 by ThreeFivePhotonics (merged with ASIP), a spinoff of the present COBRA-TU Eindhoven group. They reported a 40 channel WDM monitor chip, integrating 9 AWGs with 40 detectors. The commercial development of the chip was subsequently discontinued. The successful attempt at a commercial large scale photonic integrated chip was made in 2004 when Infinera introduced a 10 channel transmitter, with each channel operating at 10Gbit/s. This device with an integration count in excess of 50 individual components was the first LS PIC device deployed in the field to carry live network traffic. This was quickly followed by a 40 channel monolithic InP transmitter, each channel operating at 40Gbit/s per channel, with a total component count larger than 240, and a complementary 40 channel receiver PIC. As a further step in complexity, the 40 channel receiver PIC also had an integrated, polarization independent, multi-channel SOA.

3. Large Scale Photonic Integrated Circuits

Fig. 1 (upper right) shows the architecture of the 40 channel transmitter PIC. Each transmit channel consists of a tunable DFB, a back facet power monitor, an EAM, a power flattening element and a front power monitor. The 40 different wavelength channels are then combined using the AWG multiplexer. The normalized, power flattened, fiber coupled, output power spectrum of the 40 channel PIC is shown in Fig. 2. The 40 channel AWG was designed to match the 50GHz channel spacing of the DFB array.

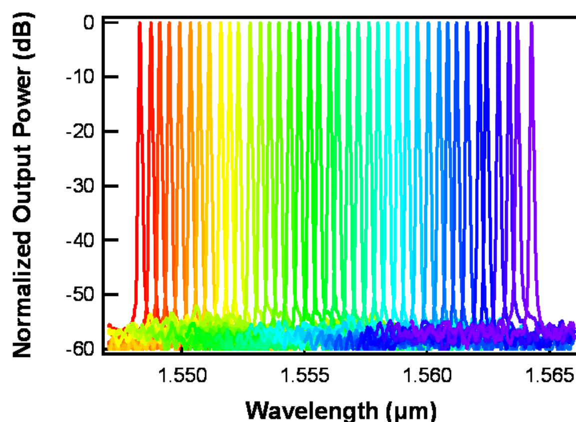

Fig. 2: Output optical spectrum of the 40 channel PIC.

Fig. 3 shows the output eye diagrams for all the 40 channels operating at 40Gbit/s. The EAM's of the PIC were individually modulated with a 40Gbit/s NRZ data stream from a pseudo-random bit sequence generator. The eye diagrams are very uniform over all 40 channels demonstrating a robust design and a high degree of control in manufacturing.

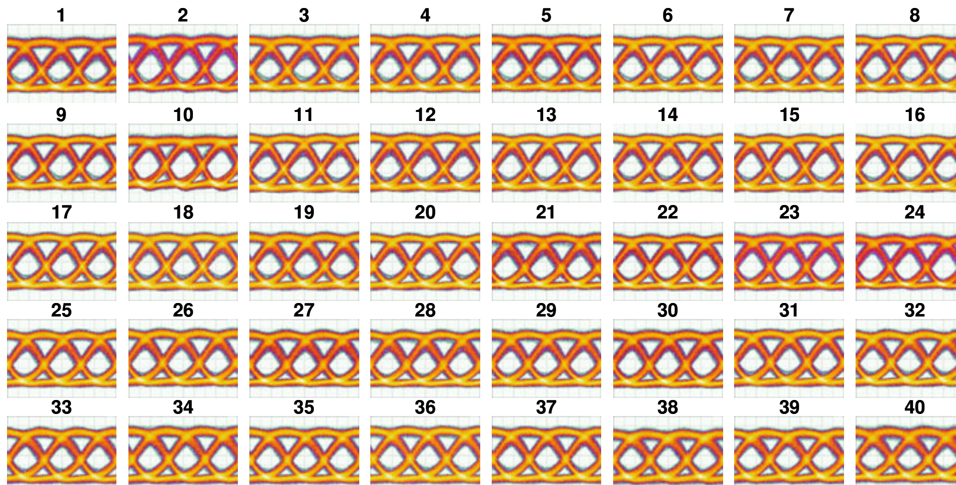

Fig. 3: 40Gbit/s NRZ eye diagrams for all 40 channels of the transmitter PIC.

Fig. 1 shows the architecture of the receiver PIC. There is a wide bandwidth SOA at the input. The 40 input channels are then demultiplexed using an AWG. The demultiplexed channels are terminated in an array of high speed, waveguide photodetectors. The SOA and AWG performances were designed to be polarization independent. The normalized, amplified responsivity of the 40 channel PIC is shown in Fig. 4. The channel spacing of the 40 channel PIC is 50GHz (for a total coverage of half the C band). Fig. 4 also shows the amplified spontaneous emission (ASE) spectrum of the SOA at 250mA bias. The -3dB width of the SOA gain spectrum is 53nm.

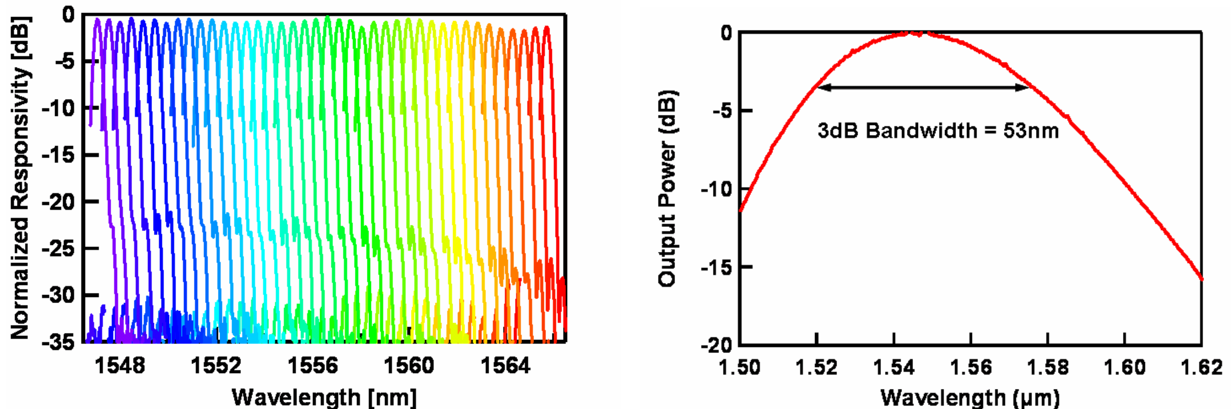

Fig. 4: The amplified optical spectrum of the 40 channel receiver PIC. ASE spectrum of the SOA at a bias of 250mA.

The median gain of the SOA is 22.7dB. The SOA's are highly manufacturable. The total variability in gain (95% to 5% of the distribution) over 300 channels is about 2.5dB. The maximum PDG over the same number devices is less then 0.8dB (95% point of the distribution) [17]. We have separately also demonstrated integrated waveguide PD with 3dB bandwidths up to 26GHz [18].

4. Data Rate Needs and Growth

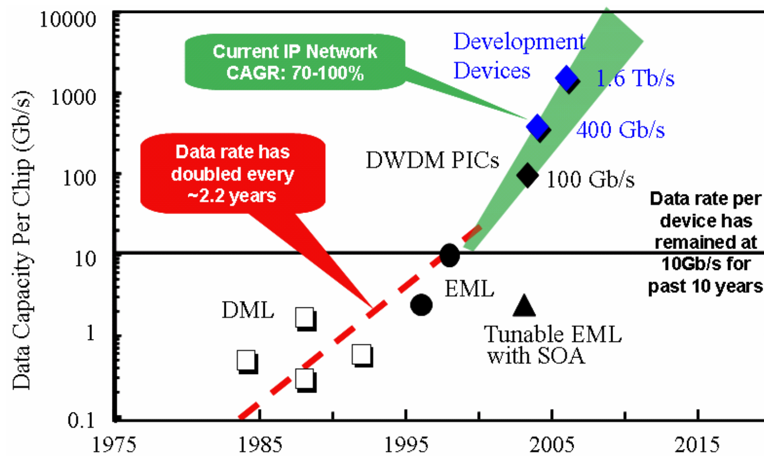

Fig. 5: Data capacity of an integrated chip in field deployment (black data points) as a function of year.

High speed optical data transport is going through a big surge. The availability of higher connectivity optical pipes closer to homes and directly to business premises is causing backbone data rates to exceed Tbit/s. Fig. 5 shows the increase in the data rate capability of single integrated InP chips, with time, currently in deployment. Despite much progress in integration, the single integrated chip data rates have remained at 10Gbit/s for past 10 years. Systems at data rates higher than 10Gbit/s were designed using external modulators until the 100Gbit/s Infinera PIC was recently deployed in the field. 100Gbit/s is also the next step in the data rate evolution of the Ethernet transmission standard, and this is being studied intensively by the IEEE 802.3 Higher Speed Study Group [19]. Integrated multi-channel, multi-wavelength solutions are serious contenders for the 100GgE implementation.

5. Beyond WDM Applications

So far, the progress in photonic integration has been hampered by the large variety in photonic devices and technologies, and the fact that most integration technologies are specific for the applications for which they have been developed. As a result, except for applications like the WDM transmission, the market for integrated photonics is too fragmented to justify the investments for developing an integration technology to a level that really leads to substantial cost reductions, and this, in turn, prevents rapid growth of the applications.

Integration processes like the one developed by Infinera, that can combine passive devices, like AWG's, with SOA's, modulators and detectors, can be used for a much broader range of functionalities than just the WDM-transmitters and receivers for which they have been developed. Examples are SOA-based WDM-switches and wavelength converters. But also time-domain applications, like ultrafast pulse lasers, that use AWGs for spectral shaping of the pulses, may be feasible.

In order to address such a broad range of functionalities the integration process has to be developed into a kind of generic integration technology that allows for well-controlled integration of a number of basic components like AWGs, MMI-couplers, SOAs, modulators (electro-absorption or electro-refraction) and detectors. If proper tools are developed or adapted for designing in such a process, without having to disclose all details of the technology, expert designers can develop many kinds of applications in such a process with development times that are much shorter as what we are used to when specific technology has to be developed for each application. This may mimic the way things are done in the micro-electronics world, and photonic integration will find broader applications beyond optical transport. This will allow for massive penetration of photonic ICs in applications like health care, sensors, metrology, consumer photonics etcetera, applications that are presently too small or to risky to justify the investments

in developing a dedicated integration process. It is a great challenge for the photonics industry to make such applications possible in the coming years.

6. What's Next?

An interesting question is how long the increase in density and complexity that is depicted in Fig. 1 will continue. On a longer term even larger channel counts then the 40 shown in the figure may occur, but it is not likely that in this way, by increasing parallelism, the complexity will exceed a component count of 1000 per chip.

The alternative is serial integration, but also along this line it is hard to envision that the 1000 components/chip barrier will be broken. The main reason for this is that today's PICs, although they usually carry digital signals, operate essentially in an analog mode. As a result, errors generated by the components will accumulate and, after having passed a number of components, the signal will be degraded so strongly that it has to be regenerated. On-chip signal regeneration is possible, but full optical regenerators are complex and they also require a significant amount of chip space. Breaking the 1000 components/chip barrier by serial integration is, therefore, also unlikely. A combination of serial and parallel integration may bring us close, but we expect that for analog PICs the increase in complexity will saturate around or below 1000 components/chip. But this is not the end of Moore's law for Photonics.

In the early days of micro-electronics analog circuits, such as operational amplifiers, formed an important market. Their complexity was typically limited to a few hundred components per circuit. Signal integrity was maintained by electrical feedback, but this limits the circuit complexity because feedback over too long distances reduces the speed and may cause instabilities. A real break-through towards VLSI required, therefore, digital circuits that operate essentially with only two levels, so that the signal is inherently regenerated after each operation and cascading of hundreds of signal operations becomes possible with virtually no signal degradation.

In photonics digital signal processing is still in an embryonic stage. A number of papers on flip-flops or logical gates have been published, but their size, speed and power consumption is such that they allow only for very small integration levels and they are by far not competitive with modern electronics. Recently a breakthrough in digital photonic signal processing has been reported by Hill [20]; a photonic flip-flop based on two coupled microring lasers with dimensions of 20x40µm^2, a switching time of 15ps and a switching energy of a few femtojoules. Its switching speed is comparable to that of high-speed electronic transistors, but its switching energy is smaller by more than three orders. This device may be used as a basis for a logical gate.

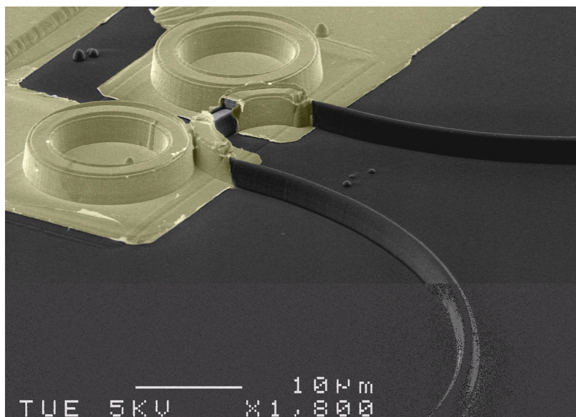

Fig. 6: Photonic Flip-Flop from Ref 20.

In comparison with electronics the photonic flip-flop is still large. In order to make it smaller the lasers have to be made smaller. Further miniaturization can be done with plasmonic lasers that have a metallic cavity [21]. Experiments show that the losses in these cavities can be overcome already at relatively low

injection current levels. Calculations show that their size can become comparable to that of modern transistors. If flip-flops and logic gates can be realized by coupling two of these lasers, in a similar way as applied for the microring laser flip-flop, then we have laid the basis for Large-Scale or even Very Large Scale digital photonic ICs.

But their potential is even larger. Because their switching power is orders lower than that of transistors, their speed is higher, and their size is comparable, they might become a contender of the transistor for ultrafast processing. For data storage their properties are less favorable, because they require the same power in static and dynamic operation. Hence, a combination of a VLSI digital photonic circuit for ultrafast processing, and a VLSI electronic IC containing massive memory, realized in an InP-on-silicon process, might extend the reign of Moore's law for electronic with another ten years. These are highly speculative and uncertain, but illustrate the new dynamics and resurgence in the photonics community.

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