

# JEPPIX

Joint European Platform for InP-based Photonic Integrated Components and Circuits

Coordinator: **David Robbins**

( [coordinator@jeppix.eu](mailto:coordinator@jeppix.eu) )

Local TU/e contact

Xaveer Leijtens ([x.j.m.leijtens@tue.nl](mailto:x.j.m.leijtens@tue.nl))

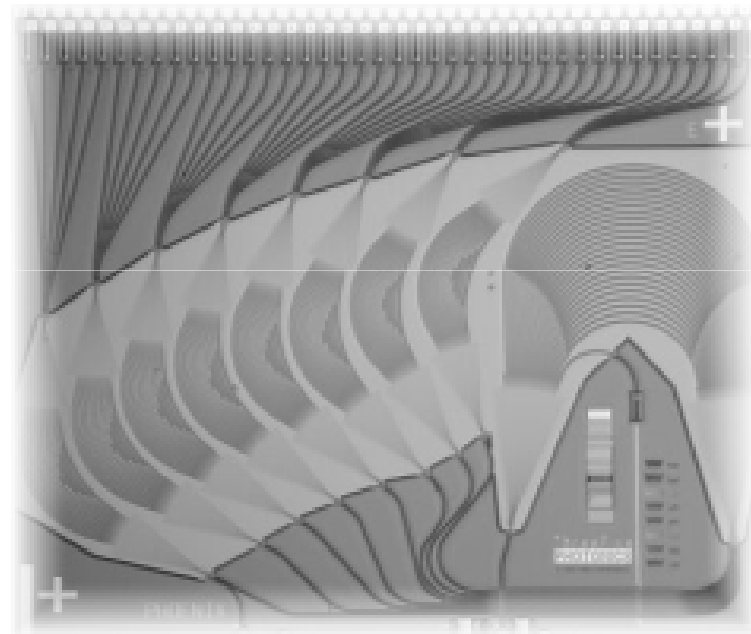


JEPPIX

Joint European Platform for InP-based Photonic Integrated Components and Circuits

# Platform Objectives

- JePPIX aims to create a solid infrastructure, offering access to Indium Phosphide based technology for proof of concept, prototyping and, long term, large volume manufacturing
- JePPIX is working to establish a *Generic Foundry* operation in an industrial fab for Application Specific InP Integrated Circuits (ASPICS)
  - A generic fab runs a fixed process with documented design rules.
  - Open to all
  - Application Blind
  - Offers large reductions in access costs to its users



40 Channel wavelength monitor chip

# Platform Partners and Users

- **User Group:** JePPIX has over 30 interested groups of potential users in Europe and has received several expressions of interest from the US
- **Application areas:** in telecoms, datacomms, sensors and medical
- **Partners within ePIXnet:**
  - *Research Institutes*
    - COBRA, Eindhoven, Netherlands
    - COM, Copenhagen, Denmark
    - KTH, Stockholm, Sweden
    - CNRS-LPN, Orsay, France
    - Alcatel-Thales III-V lab, France
  - *CAD Design*
    - Phoenix, Enschede, Netherlands
    - Photon Design, United Kingdom
    - Politecnico di Milano (POLIMI)/Filarete
  - *Chip manufacturers*
    - Bookham, United Kingdom
    - CIP, United Kingdom
    - Cedova, Eindhoven, Netherlands
    - FhG-Heinrich Hertz Institut, Germany
    - CST/Photonix, UK
  - *Equipment manufacturers*
    - AIXTRON, Aachen, Germany
    - ASML, Veldhoven, Netherlands
    - OPT, Yatton, United Kingdom



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# Platform Technology

- Photonic Integrated Circuit Fabrication:
  - The JePPIX platform currently offers access to an InP-based active/passive integration process at the COBRA fab (TU/e) for research and prototyping
  - The platform offers a number of elementary building blocks: Gain sections, phase contral sections and shallow and deep etched passive waveguides
  - Each process run is on a best efforts basis
  - COBRA is *path-finding* InP integration technology for generic fab operation
- Wafer runs are shared between users
  - ASPIC Design and technology training provided by TU/e
  - ASPIC Design Support offered to JePPIX users
  - Post fabrication testing to validate wafer processing undertaken at TU/e
- JePPIX is working with its industrial partners
  - to address how to move the platform onto an industrial process with
    - high performance
    - reduced access costs
    - long term viability
    - proven long term device reliability

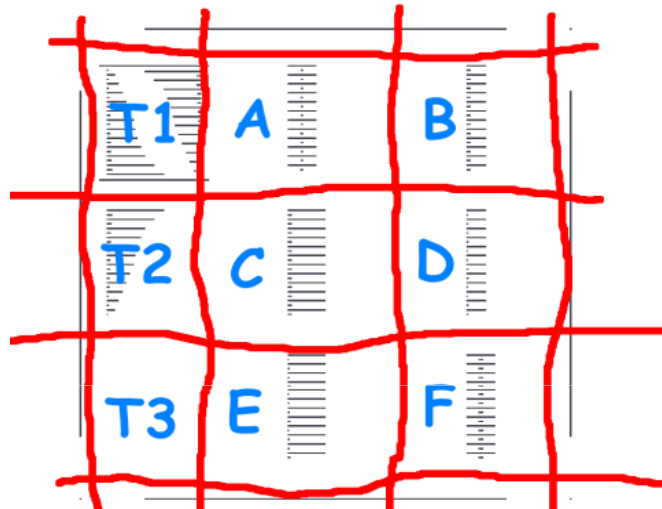


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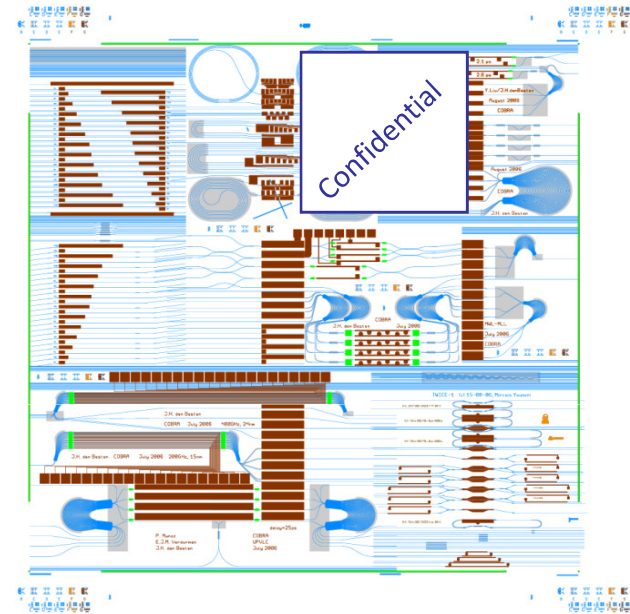
# Multi-Project Runs

The processed area is split into nine blocks (typically 4x4mm<sup>2</sup>); three of which are reserved for test structures (to qualify the processing) and six blocks host the designed PICs of the users.

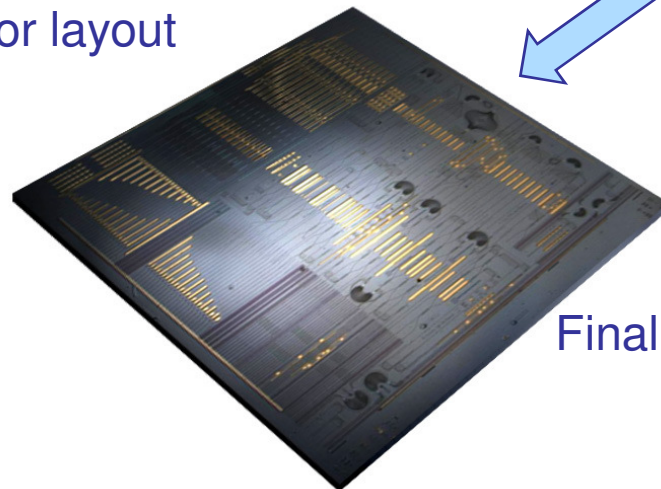
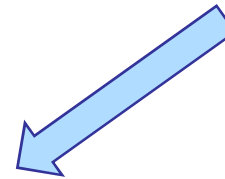
Test Sectors T1-T3 for wafer scale verification



Sector layout



Mask layout (JePPIX\_1)



Final Processed Circuits



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# JePPIX in ePIXnet

- JePPIX\_1 chips being assessed by users.
- JePPIX\_2 in fab
- JePPIX\_3 in design (last ePIXnet shared wafer run)
- Cross Platform Coordination
  - JePPIX is working with the packaging platform (EpixPACK) on a packaging solution for InP ASPICs
  - Participation in an ePIXnet platform workshop end February

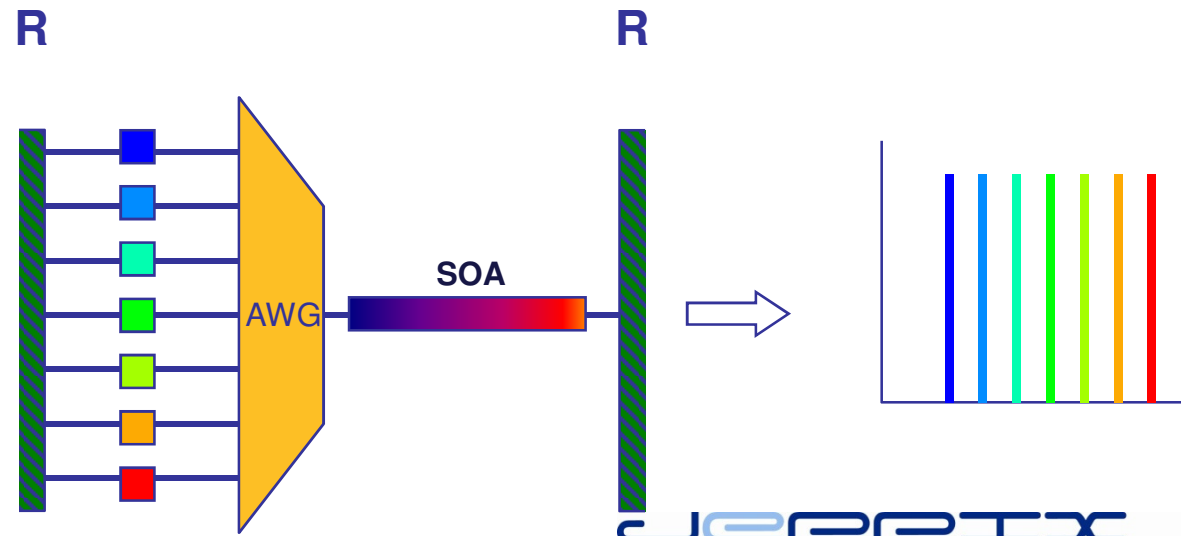


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# Example of fabricated circuits: Multi-Wavelength Laser



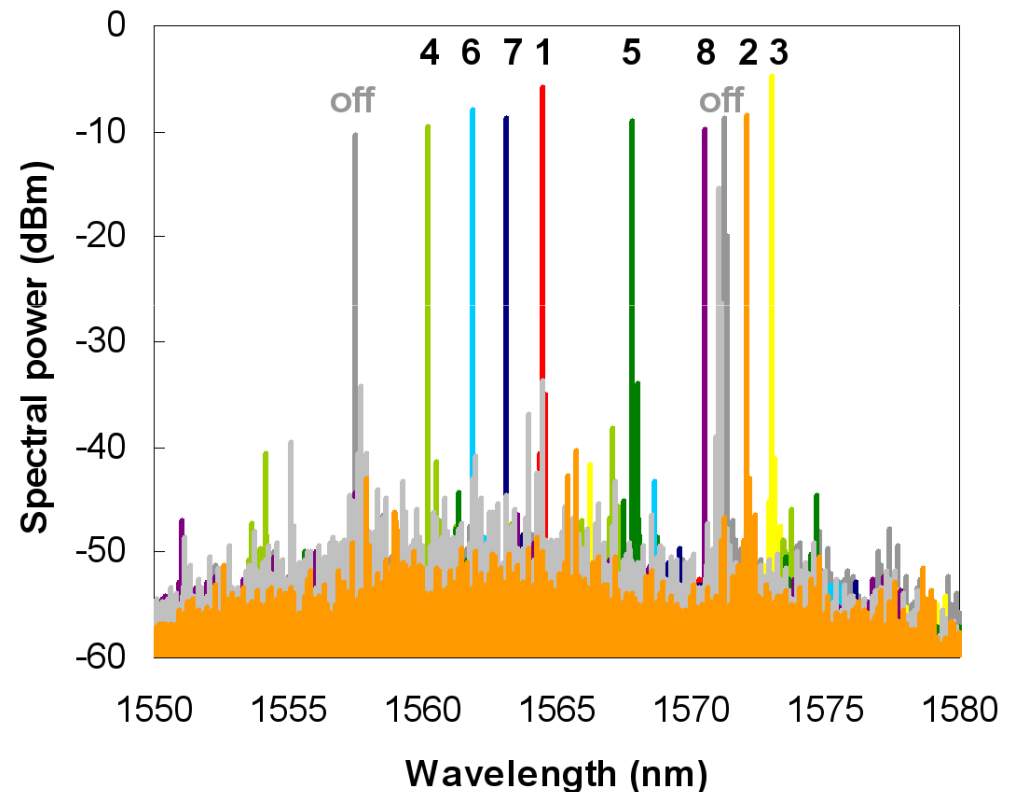
- SOA Gain
- AWG
- Passive waveguides



# Example of fabricated circuits: Multi-Wavelength Laser

X Leijtens et al. LEOS PD'08

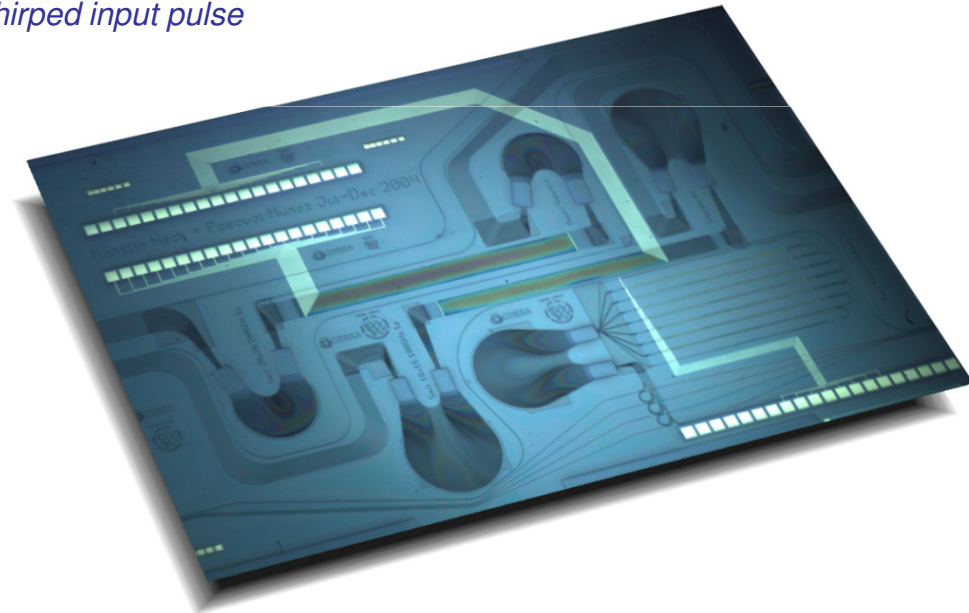
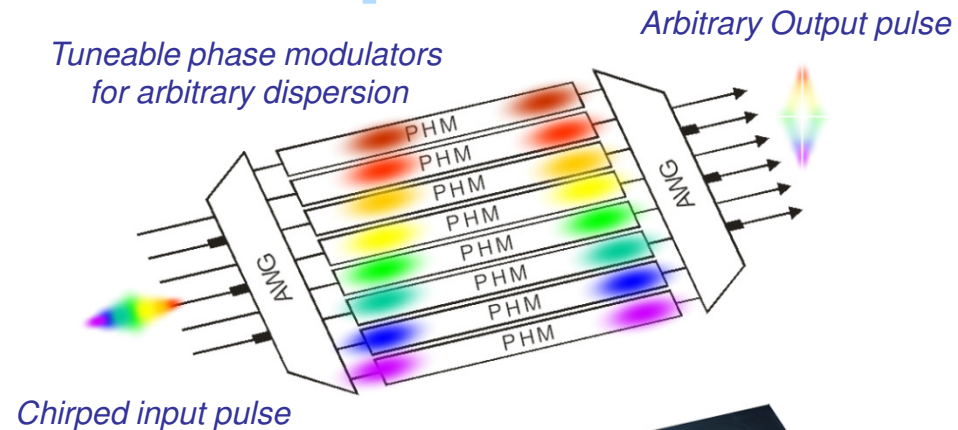
P Muñoz Muñoz - This meeting



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# Example of Fabricated circuits: Pulse Shaper

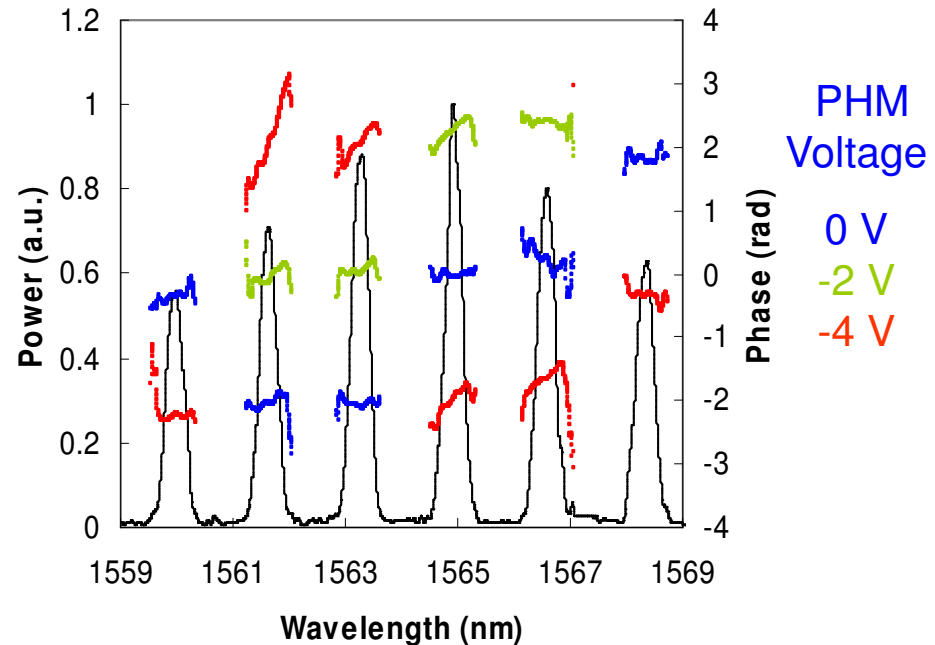
- Spectral phase control of short optical pulses  
~1550nm
- Complete arbitrary pulse generator is possible
  - Phase Modulator
  - Passive Waveguides
  - AWG.



# Example of Fabricated circuits: Pulse Shaper

Martijn Heck, Pascual Muñoz  
Muñoz et al., LEOS '07 and  
J. of Quantum Electronics,  
p370 QE44(4) April 2008

- Applications in telecommunications
  - dispersion (pre-) compensation and arbitrary waveform generation.
  - Coding technologies such as optical code-division multiple-access (O-CDMA),
  - Bio-imaging, using second harmonic pulses for multiple photon excitation



- Pulse reconstruction of 0.3ps pulses demonstrated
- Dispersion compensation of up to 0.2ps/nm possible.



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# JePPIX after ePIXnet

- Short Term
  - Fabrication runs – one per year at COBRA
  - R&D level platform access on a best efforts basis
  - Continued user support in ASPIC design and in Technology Training
- Longer term JePPIX must address how to develop a service for both commercial and R&D users which can be self-sustaining
  - The JePPIX *user group* is a key instrument for new users to gain platform access and for the platform to gain access to new markets
  - Join our *user group* if you think JePPIX can be of help to you
  - **EuroPIC** – programme “above threshold” in the recent NMP3.5.1 call
    - partners HHI and Bookham propose to establish generic process platforms
    - first generic foundry run at an industrial facility 2012
- New programme bids into FP7 and national schemes – ICT Call 5



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# Platform Impact

- JePPIX aims to provide Europe with a strategic advantage in photonic integration
- What can JePPIX achieve?
  - Market restructuring around a generic fab capability
  - Increased wafer volumes through fabs
  - Reduced cost of entry into the technology for new users
  - Cost reduction for all low to medium volume fab users
  - Rapid prototyping and validation of products with proven reliability
- JePPIX aims to stimulate associated market sectors i.e. *Design house* specialists skilled in ASPIC design at the circuit level
  - Improved accessibility to the technology for all
- Europe has a lead over the US and Far East – work to preserve that advantage.

