



JePPIX

Joint European Platform for InP-based Photonic Integrated Components and Circuits

Coordinator: David Robbins (coordinator@jeppix.eu)

Local TU/e contacts:-

Fouad Karouta (f.karouta@tue.nl)

Xaveer Leijtens (x.j.m.leijtens@tue.nl)

ePIXnet Annual Meeting
6-7 September 2007
www.epixnet.org

Starting Point

The key bottlenecks in photonic integration on InP

- (By far too) many degrees of freedom
 - many different materials and technologies
 - many different component types
 - many different wavelength ranges and applications
- Furthermore:
 - total cost of ownership of a wafer fab is very large
 - most photonic markets still have only moderate volume
 - a very high level of expertise is currently required to design on those processes
- Hence:
 - most companies cannot afford their fab.
 - and most venture capital is unwilling to build new fabs



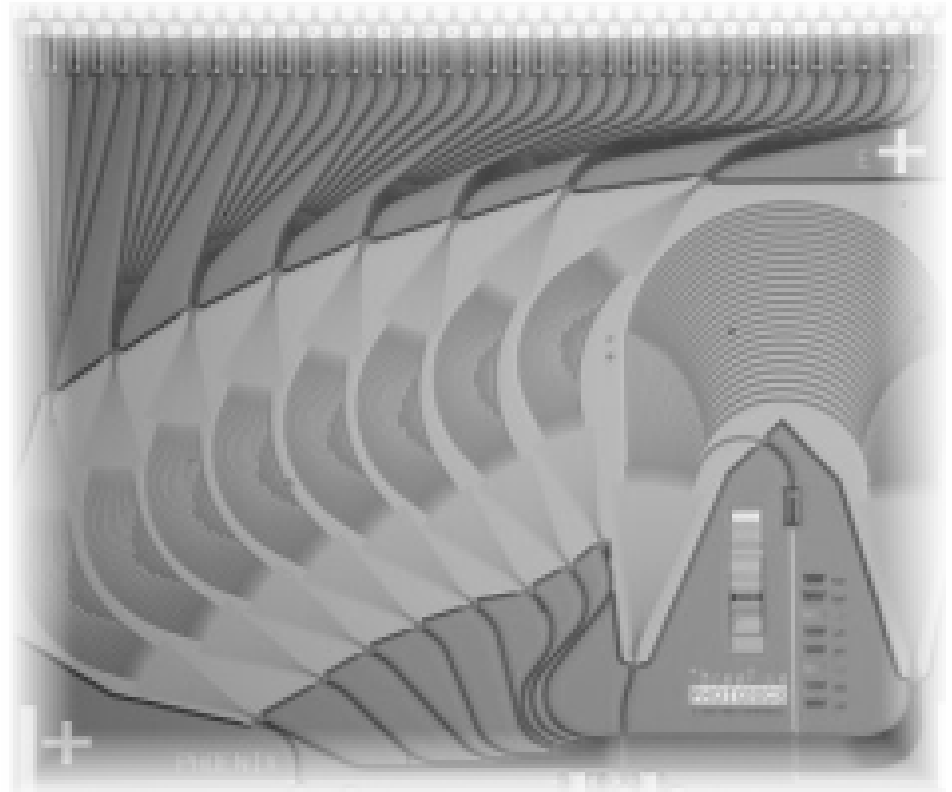
The ePIXnet solution

- Develop a **limited number** of generic wafer-scale **integration technologies**, that can support a **broad range** of functionalities and applications
- Move to a **foundry model**
 - Convergence of technologies
 - Decouple design (IP) from technology (IP)
- These challenging initiatives address access to existing facilities
- They do not address the overcapacity in the components industry which still needs to restructure.



Joint European Platform for InP-based Photonic Integrated Components and Circuits : JePPIX

- JePPIX aims to provide Europe with a strategic advantage in photonic integration. Europe's key industrial and academic players are joining forces to create a solid infrastructure, offering access to Indium Phosphide based technology for proof of concept, prototyping and, long term, large volume manufacturing.
- Partners:
 - Research Institutes
 - COM, Copenhagen, Denmark
 - KTH, Stockholm, Sweden
 - CNRS-LPN, Orsay, France
 - COBRA, Eindhoven, Netherlands
 - FhG-Heinrich Hertz Institut, Germany
 - Chip manufacturers
 - Bookham, United Kingdom
 - CIP, United Kingdom
 - Cedova, Eindhoven, Netherlands
 - III-V lab, France
 - 3S Photonics, France
 - Svedice, Sweden
 - CST/Photonix, UK
 - Equipment manufacturers
 - AIXTRON, Aachen, Germany
 - ASML, Veldhoven, Netherlands
 - OPT, Yatton, United Kingdom
 - CAD Design
 - Phoenix, Enschede, Netherlands
 - Photon Design, United Kingdom
 - Politecnico di Milano (POLIMI).
- Users
 - ePIXnet: UPVLC (E), POLITO (I), IMEC (BE), Cambridge (UK)
 - non-ePIXnet: ENST (FR)

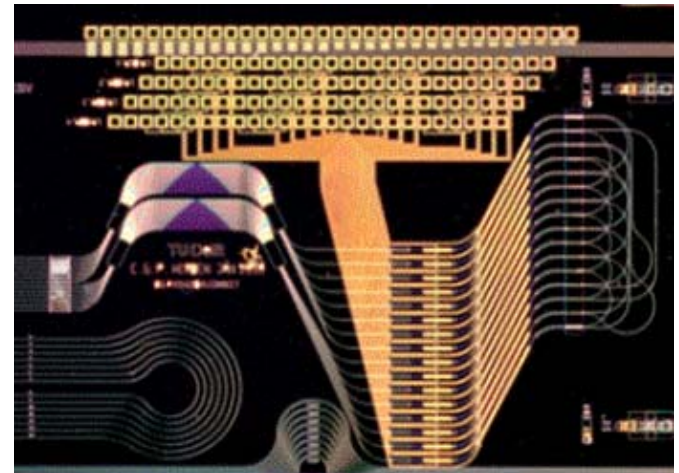


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Platform Tasks

- The platform addresses:
 - Research and Prototyping
 - ▶ Access to Photonic IC design and fabrication for SME's and research institutes
 - ▶ Generic integration technology development
 - Innovation
 - ▶ Compatibility of academic and industrial processes
 - ▶ Launching start-ups
 - ▶ Launching a foundry
 - Education
 - ▶ Training in photonic IC design and technology



4-wavelength optical crossconnect

Infrastructure - what is offered within ePIXnet

Access to an InP-based active/passive integration process (SOAs, MMIs, AWGs) for research purposes on a best effort basis.

- PIC Design & technology training (2 weeks)
 - Once a year
 - Cost: 4000€
 - Free for ePIXnet members
- PIC Design Support
 - Cost 150€/hr
 - Free for ePIXnet members
- PIC Fabrication
 - 2 runs per year, 2 wafers per run (1/4 of 2")
 - 6 sectors per mask design
 - Cost: ~60,000€ per run
 - ▶ i.e. ~10,000€ per chip or 600€/mm²
 - Charged to ePIXnet members:
 - ▶ 2,000€ per sector or 120€/mm² if chips are within an agreed spec.



Response to reviewer feedback

- **EPIXNET annual review 2006 - feedback on InP platform**

“ This [*technology platform*] structure in itself is already recognised as a significant integration achievement, and it is likely to facilitate further collaboration within the project and beyond”

“All targets are basically met apart from the device characterization by industrial partners.”

“Fabrication yield (high losses) and limited chip performance related to instability of processing..... a characteristic problem of a university environment and is addressed.”

“...clear industrial vision in writing on how to achieve this goal is lacking.”

- **Response is to fully involve the industrial fabs.**

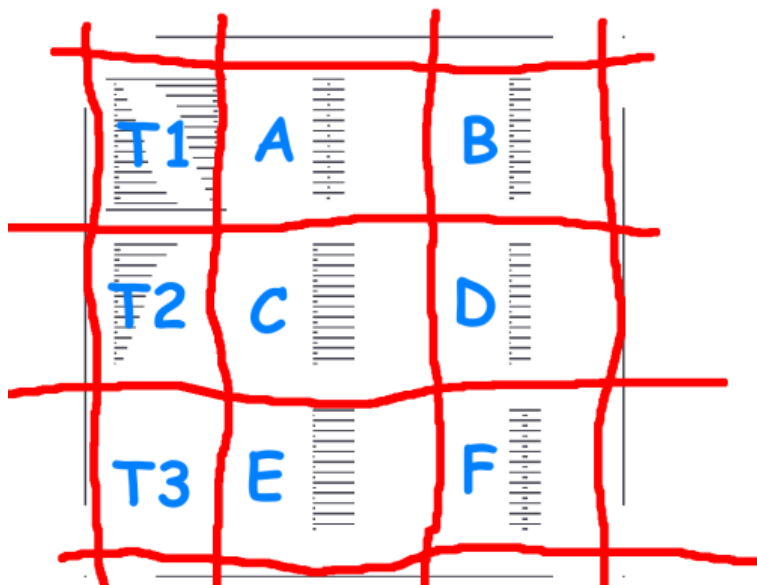
- **Industrial participation in JePPIX furthered by three JePPIX consortium meetings**

- Common philosophy and consensus
- Submission of an IP and a CSA into FP7
 - ▶ consolidate the present position
 - ▶ move forward with foundry fab. technology and applications
 - ▶ secure the future of JePPIX



Sectors on the JePPIX and FAA1 masks

TU/e COBRA ACTIVE PASSIVE 01 2005
ACTIVE #1



T1-T3 test and validation areas

Areas A-F user designated sectors

ePIXnet MASK SET 2, M050929



Highlights - ePIXnet FAA1

- Multi-user run 3 (mask set #2)
 - 7 PICs in the design.
 - Circuit building blocks offer planar waveguides, semiconductor optical amplifiers, phase modulators
 - No highlights yet (see later slides)
- Rerun Multi-user run 1
 - Successful demonstration of AWG-based pulse compressor chip, cooperation UPVLC-COBRA
Paper submitted to JQE
- Compatibility demonstration:
 - Epitaxial structure grown by CIP
 - processing by COBRA in JePPIX AP-process
 - Chip demonstrated in IST MUFINS project



FAA1- Issues

Modifications of the JePPIX Active/Passive process in 2006/7

- Addition of process steps for supporting integration of phase shifters
- Modification of the planarisation procedure in order to support contacting of mesas with widths smaller than $3\mu\text{m}$ – significant effort to develop new self aligned process.

Problems encountered

- Despite of succesful test runs FAA1 ran in 2006/7 failed due to high waveguide propagation losses:
 - Chips still awaiting assessment at Cambridge
 - Response:
 - Process problems identified and probably solved, final tests will be fnished shortly
 - Introduction of phase shifters postponed
 - FAA1 designs, if still relevant, will be transferred to JePPIX run 2 (scheduled April 2008) if e-o phase shifters are available.
- Loss of a COBRA processing technician to a JePPIX partner
 - Response:
 - Recruit or train to backfill
 - In the meantime reduce number of runs from three to two / year
- ePIXnet funding for the COBRA efforts is far less than marginal (<20%)
 - Response: in future projects reserve sufficient funding for COBRA efforts



Highlights – JePPIX

- JePPIX Symposium 30th Nov 2006
 - ~100 attendees, 40% industrial)
- 2-weeks PIC Design and Technology Training Nov 2006,
 - 7 attendees
 - 4 attendees went on to produce designs for JePPIX run1
- First JePPIX multi-project fab run using mask set JePPIX_1 containing PICs for
 - CAM (JRA –Short Pulses)
 - UPV (Valencia) (JRA AWG Based devices)
 - Polito Torino (JRA AWG Based devices)
 - COBRA (3x)

Processing scheduled to commence October 2007

- Most of Europe's key players in the field of research, PIC and equipment manufacturing and Photonic CAD are participating
- Preparing an FP7 IP that has the ambition and the potential to bring Europe at the forefront of Photonic Integration



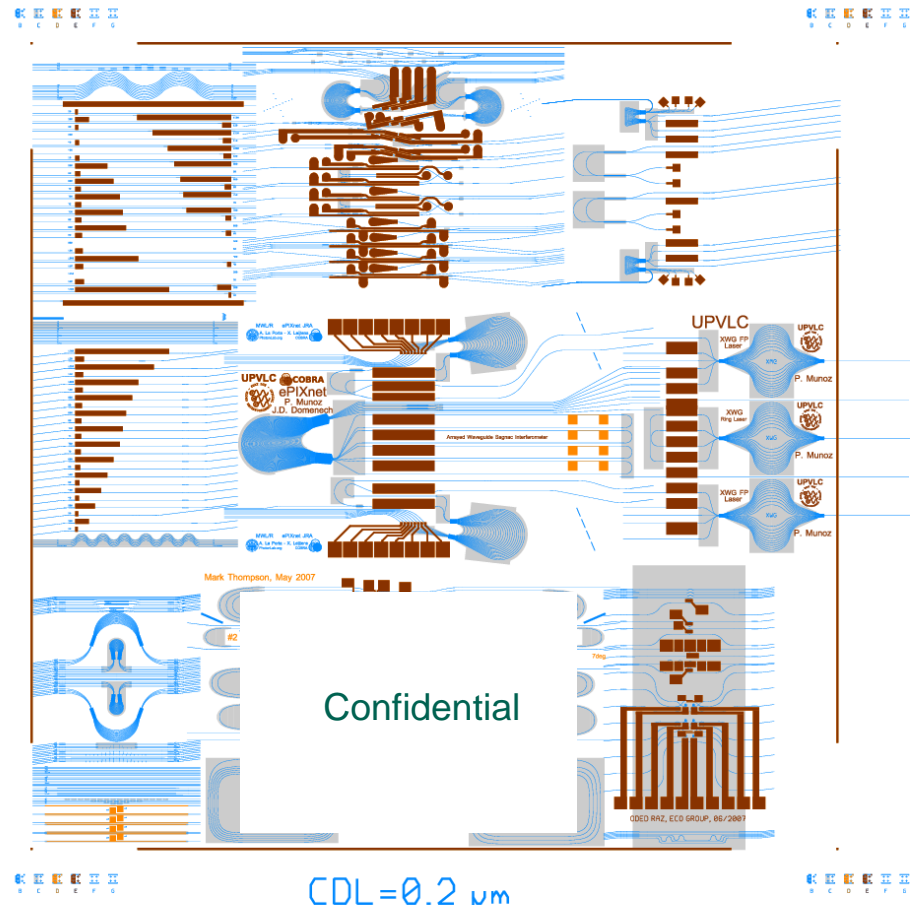
JePPIX run 1 layout

Mask in the final stages of completion.
Process run October '07

- A - COBRA/Cambridge
- B - COBRA
- C - Torino/COBRA and UPVLC/COBRA
- D - UPVLC
- E - Cambridge
- F - ECO/COBRA

JePPIX 2007-01, M070601

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Lessons learnt so far

- One month originally scheduled for chip design appears to be too short for a beginner designer
 - Response: increase design period to three months and total cycle time (incl fabrication and characterisation) to 6 months, i.e. 2 runs per year
- Concentration of JePPIX training and COBRA-based design support in a 6 weeks period appears to be impractical
 - Response: organise remote support and a “come-back” week shortly before closing of mask file submissions.
- Mask layout tools enhanced at COBRA to facilitate compilation of multiple cells from multiple sources
 - Design rules for matching across sectors on the wafer need revising
 - Support required at COBRA in mask design and realisation significantly underestimated
- Test structure validation successful



Plans for the future

2007/2008

- Symposium for outreach to users
 - First symposium in Netherlands successful – repeat at a different European venue
- Two week PIC design & Technology Training (starting November 12th, 2007)
- Continued PIC design support
- Two fabrication runs (starting in October 2007 and April, 6 PICs per run)
 - Only SOA and PWD (MMI and AWG, deep and shallow)
- Submission of FP7 Integrated Project and Submission of FP7 CSA (jointly with silicon photonics platform)
 - First access to industrial process early 2009.
 - Convergence of generic technologies at partners
 - Foundry process with proper design interface available before 2013
- Preparation of STREPs
- Preparation of Technology Roadmap



JePPIX Events for your Diary

- **Training course in mask design running at TU/e
November 12 – 23rd 2007**

1st week: Design of Photonic Circuits
Lectures and practical training with design software

2nd week: Photonic Integration Technology
Lectures, training in the clean room and practical studies on the optical measurement of InP-based passive waveguides

- **JePPIX platform fabrication run 2 is planned to commence in April 2008**

**14th European Conference on
Integrated Optics
Eindhoven, The Netherlands, June 11-13,
2008**

