Low cost packaging for high optical port counts

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CIP

InP Foundry Services

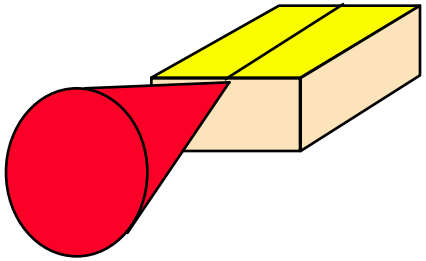
- Objective
  - Wide range of designs
  - Multi-project wafer runs
  - Monolithic integration
- Need for package simplification and standardisation to reduce cost

Approach

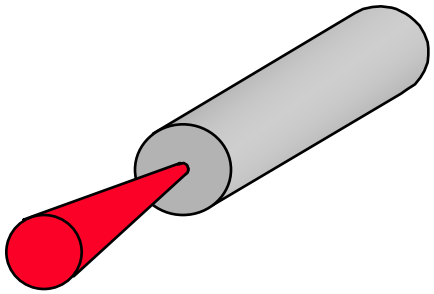
- Standardise
  - Chip sizes
  - Positions of optical interfaces
  - Mode sizes of optical interfaces
  - Positions of RF interfaces
  - Positions of DC interfaces

Fibre coupling

- Need to match active optical mode size to fibre mode ~ 8um
- Active devices have small modes ~ 1um
  - Small mode + lensed fibre
    - tight position tolerances
  - Mode converter on active + cleaved fibre
    - relaxed positional tolerances

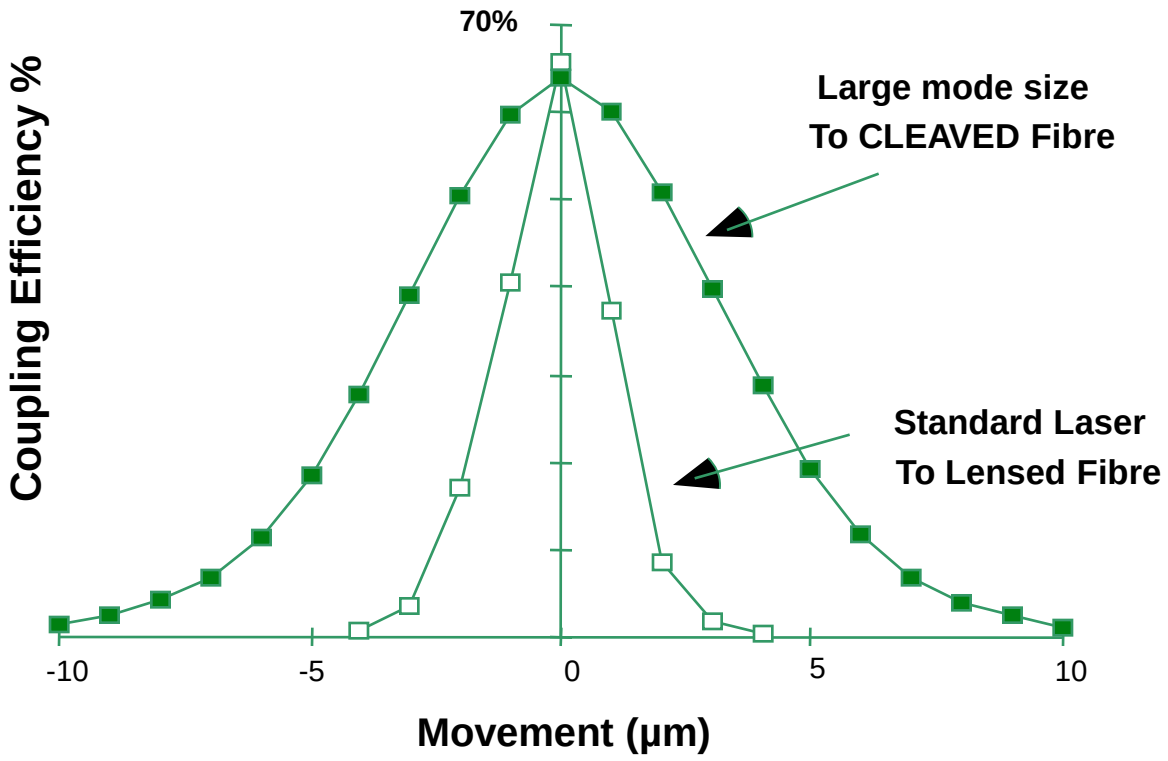


Laser Farfield
30 ° by 40 °



Fibre Farfield
7.5 ° by 7.5 °

Alignment Tolerances

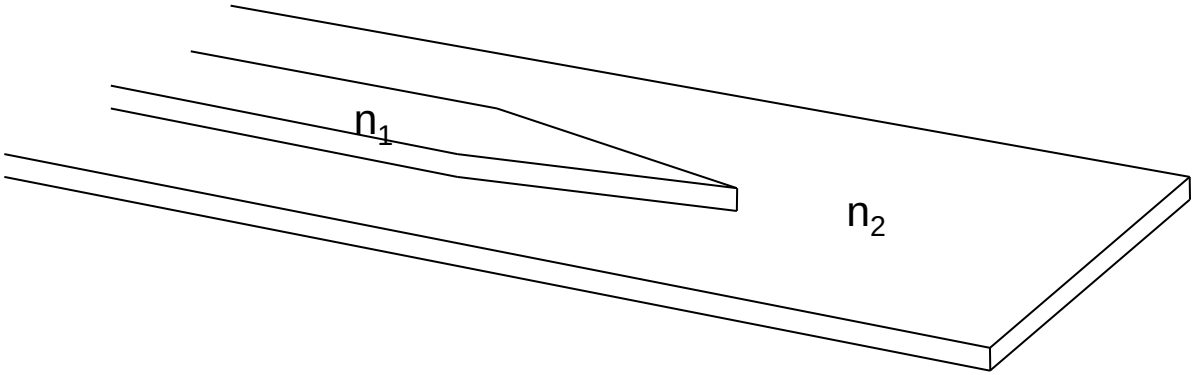


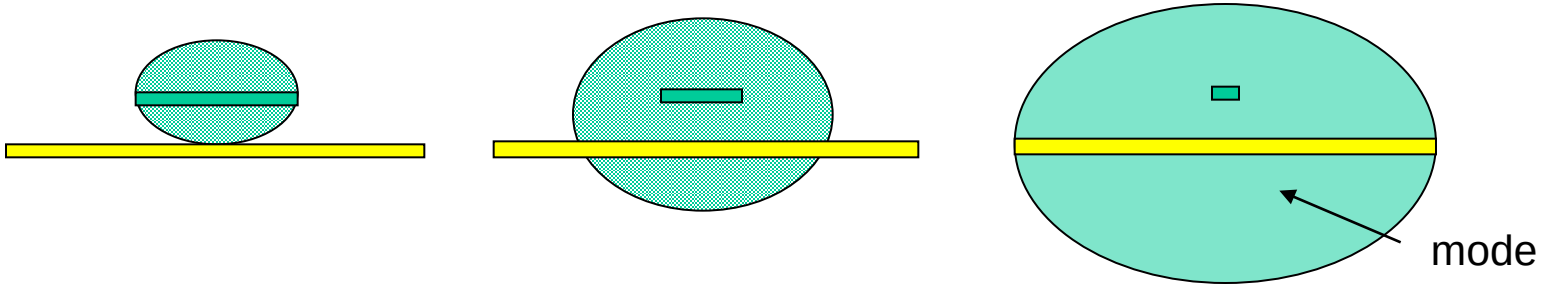
Collins et al., OFC ‘95

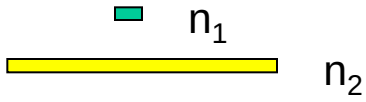
Mode size

- Small
  - Small bend radius
  - Bad x,y,z coupling tolerance
  - Large free space diffraction angle
- Large
  - Poor bend radius
  - Good x,y,z coupling tolerance
  - Low diffraction angle
- 1dB loss for offset of ¼ mode diameter
- 4dB loss for offset of ½ mode diameter

Buried waveguide mode transformation



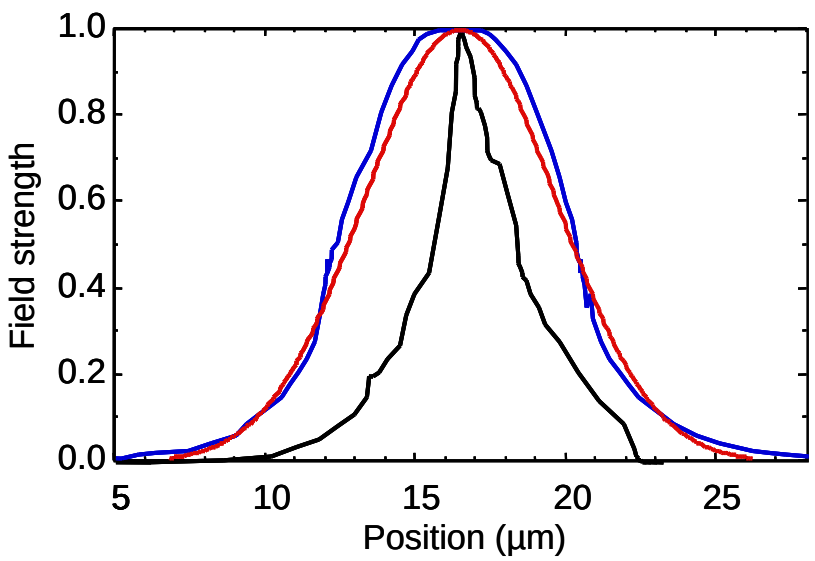


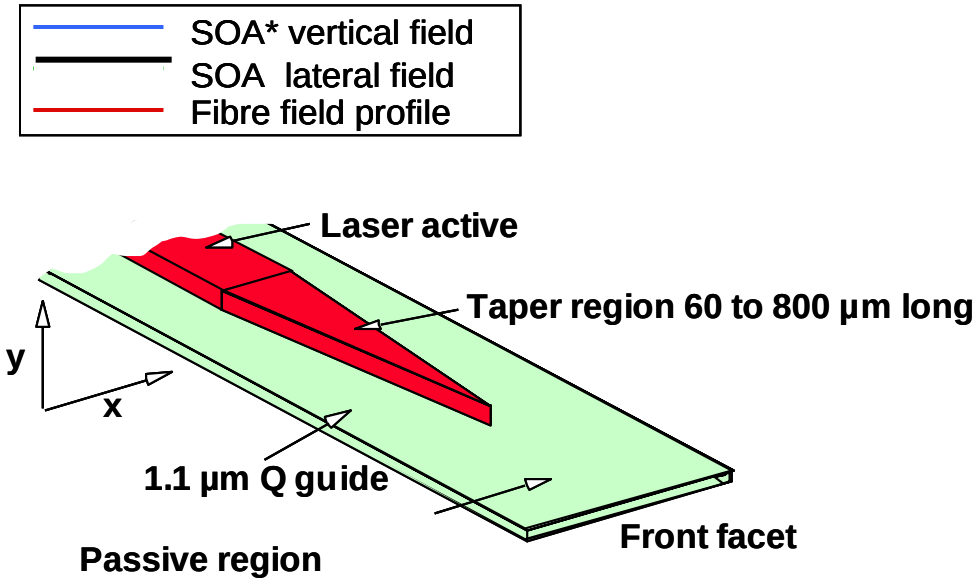


Where $n_1 > n_2$

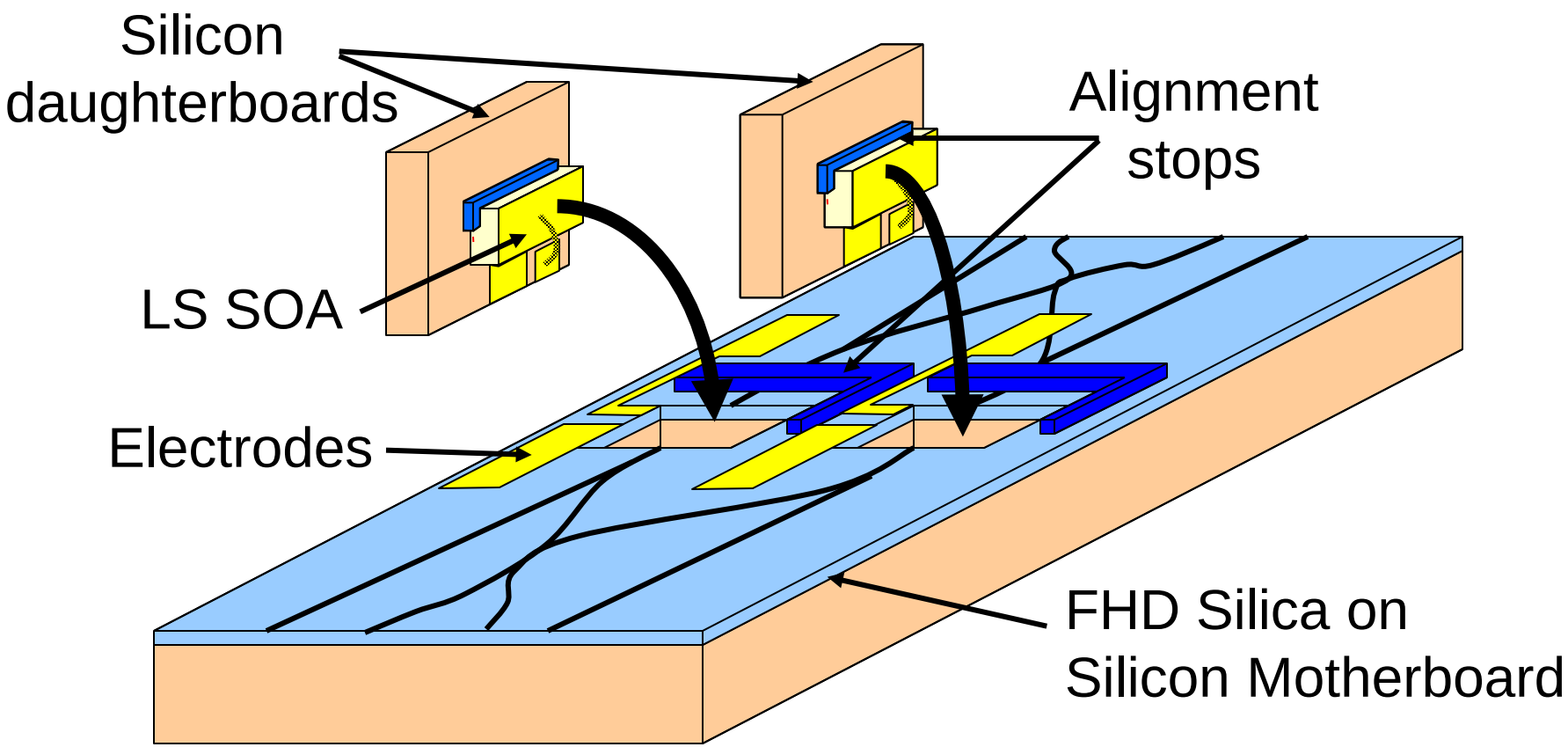
Semiconductor Amplifier Arrays

- SOAs are mode expanded ~ increases tolerance to misalignment
- Farfield angle in air is ~ 8 by 12 degrees
  - Profiles compared to 10 micron SM fibre



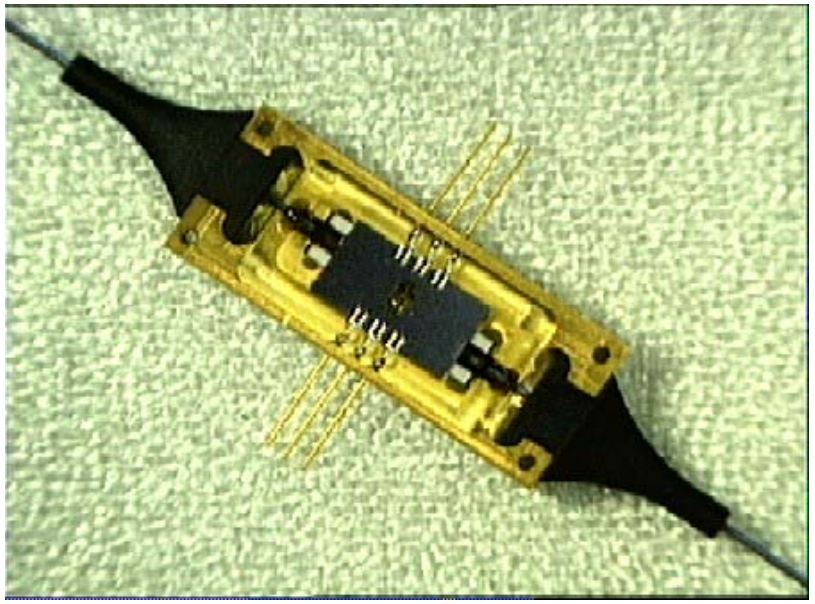


Hybrid MZI Schematic



3rd generation hybrid assembly example

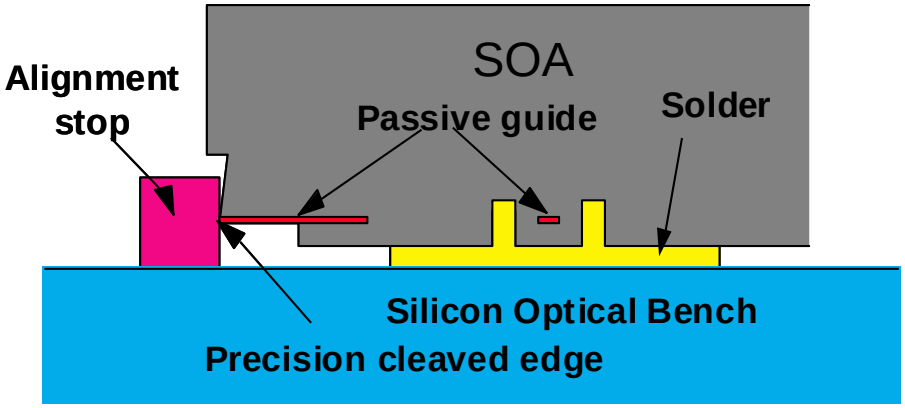
- Design example is for a quad assembly of SOAs on to a planar silica motherboard containing waveguides
- Mode expanded, precision cleaved SOA array
- Waveguides are 0.75% delta, 5x5um with tapers up to SOA and fibre interfaces
- Passive assembly of SOA on to silicon submount (daughterboard) and passive assembly of daughterboard on to passive waveguides (motherboard)
- Devices tested at each assembly stage, motherboard tested prior to machining of hole.

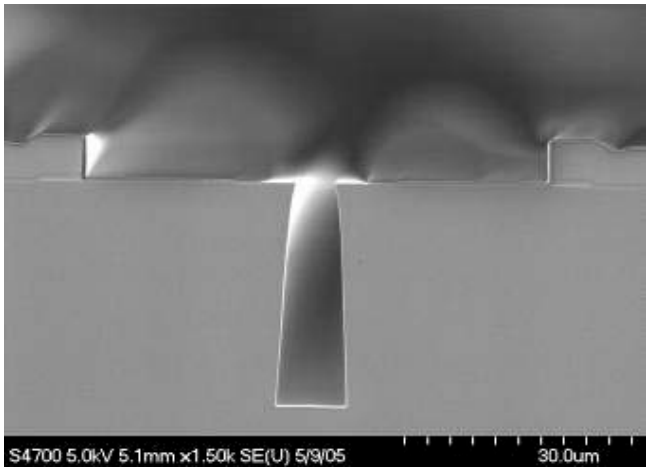


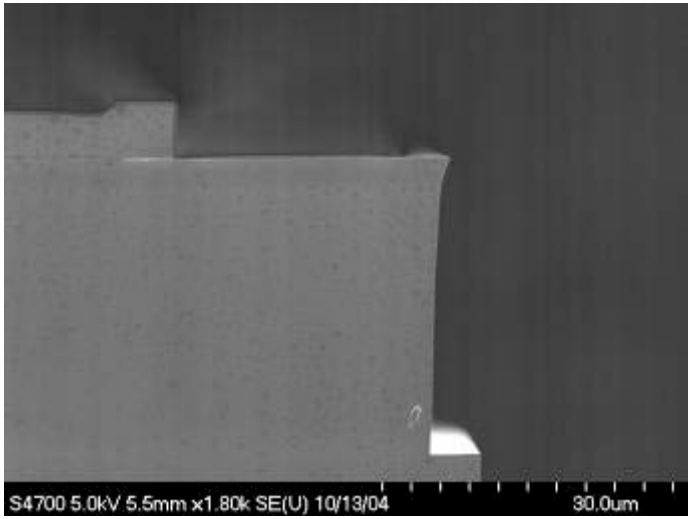
Packaged quad hybrid

Precision Cleaved Non-linear SOA Twin

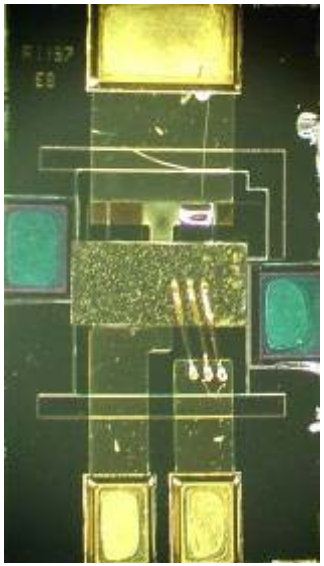
- Passive waveguide layer acts as an etch stop.
  - Lithographically positioned relative to the SOA output guide

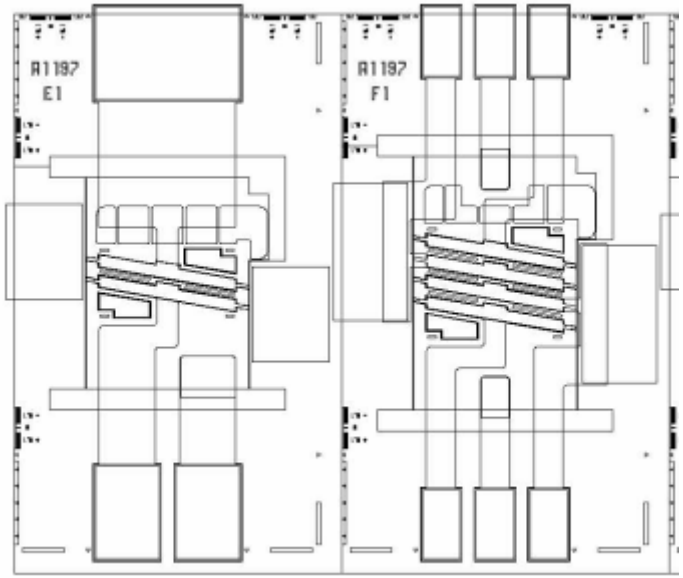






Silicon Daughterboards

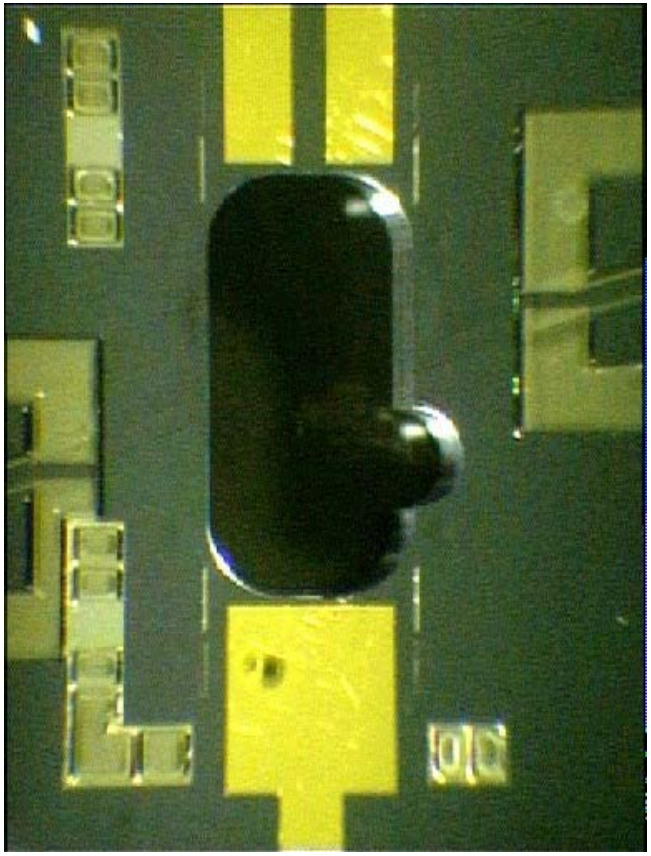




- Micromachined silicon daughterboard
- Passive flip-chip assembly of SOA array against mechanical end-stops
  - Test chip on submount and burn-in at this stage
- Precision edges of submount passively assembled on motherboard against end stops

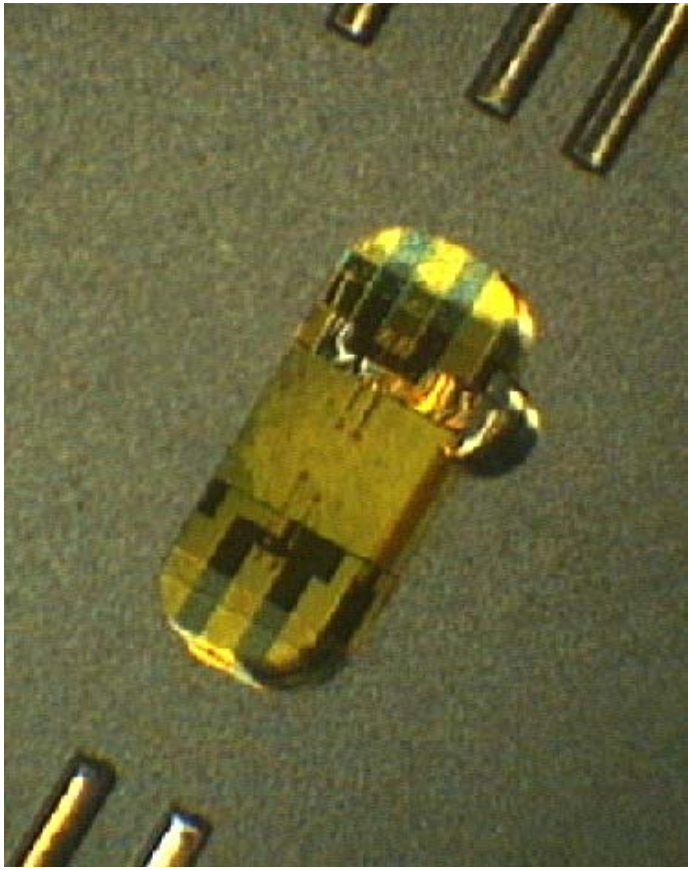
Detail of milled hole

- Hole is precision machined in motherboard
- SU-8 used as mechanical alignment feature on both motherboard (shown) and daughterboard



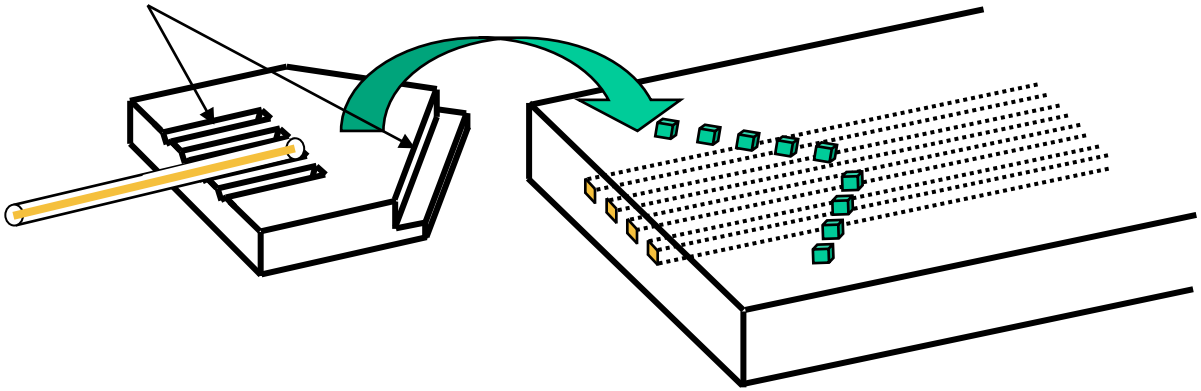
Assembled Hybrid

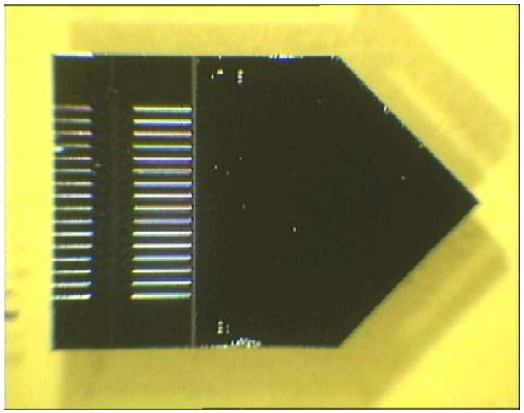
- Daughterboard containing SOA array assembled on to the motherboard
- Passive assembly of precision daughterboard against end stops on motherboard
- Index matching gel fills the gap between active and passive device



Passive Pigtailing

Wet etched faces & V-grooves



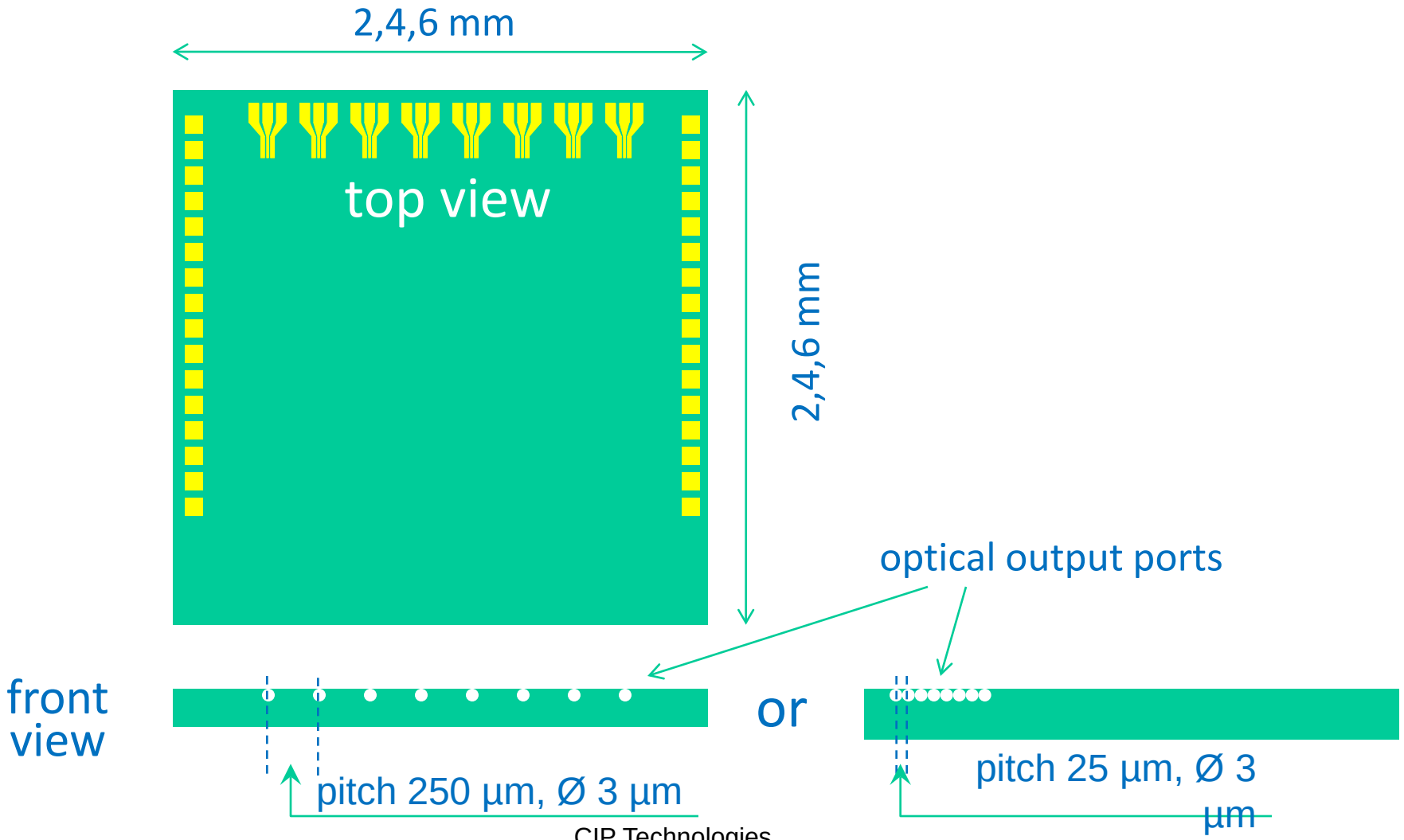


CIP Hybrid Integration Platform

- Four component parts
  - Active device (SOA)
  - Daughterboard (Si)
  - Motherboard (PLC)
  - Fibre array pigtails
- Overall device designed together as a hybrid
  - not separate components ‘bolted’ together
- Components push together against precision alignment stops (passive assembly) with ~ µm alignment tolerance
  - a prerequisite for low cost
- Uses ‘end-fire’ optical coupling between components (in-plane)
- Designed to allow outsourced manufacture

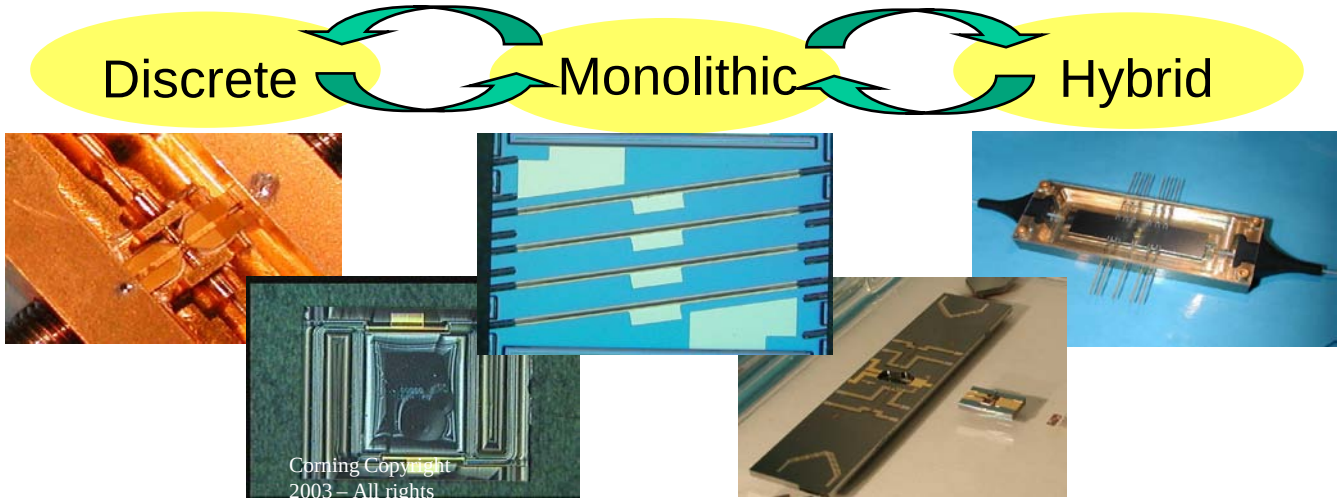
PARADIGM PIC

- **standardized e/o port positions (draft)**



CIP Integration Vision

- Realisation of the ‘photonic circuit board’
- A scalable integration platform for different materials & devices
  - Migration to more complex and larger scale sub-systems, 3D integration
  - Standardisation extended across technology platforms
- Monolithic and hybrid integration balance
  - Optimum will shift with time as technology advances
  - Need expertise in both



Conclusions

- Offers a scalable approach for devices with multiple optical interfaces
- Costs scale sub-linearly with channel count
- Standardisation of chip size, interface positions and mode sizes